invention, a graphic driver responding to an application program may set up data structures (preferably in local memory 21) which describe a large portion of memory (system or local) in which particular texture maps may be stored. The kernel driver obtains page tables from the operating system and uses these to provide page table entries (PTE) 24 in each data structure giving the physical addresses of texture map data in memory (system or local). The kernel driver then provides a reference to allow the direct memory access (DMA) engine 19 top access the data structures and find the portion of memory in which the texture maps are stored in response to application commands. The kernel driver may store the page table entries 24 in local memory 21 so that the DMA engine 19 may accomplish virtual-to-physical address translations locally.--

In The Claims

Please cancel claims 42-61, 70-81, and 90-99 without prejudice or disclaimer.

Please add new claims 100-112 as indicated below. No new matter is added.

100. (New) A computer system, comprising:

a bus;

a central processing unit coupled to said bus; and

a graphics accelerator coupled to said bus, said graphics accelerator including a texture cache system, said texture cache system including a texture cache memory that stores texels to be used by a texel value generating circuit, a cache controller that performs a replacement policy determination for texel data to be stored in said texture cache memory, and a direct memory access engine that retrieves texel data from memory, wherein said replacement policy determination operates such that a common priority scheme is applied to a plurality of cache lines containing texels.

101. (New) The system of claim 100, wherein said replacement policy determination is performed using at least one set of flags that are associated with the plurality of cache lines.

102. (New) The system of claim 100, wherein the plurality of cache lines number sixty-four, and wherein each of the plurality of cache lines stores sixty-four texels.

103. (New) A computer system, comprising:

a bus;

a central processing unit coupled to said bus; and

a graphics accelerator coupled to said bus, said graphics accelerator including a texture cache system, said texture cache system including a texture cache memory that stores texels to be used by a texel value generating circuit, a cache controller that performs a replacement policy determination for texel data to be stored in said texture cache memory, a local memory, and a direct memory access engine that retrieves texel data from memory, wherein said direct memory access engine implements a virtual-physical address translation based on page table entries stored in the local memory.

104. (New) A computer system, comprising:

a bus;

a central processing unit coupled to said bus; and

a graphics accelerator coupled to said bus, said graphics accelerator including a texture cache system, said texture cache system including a texture cache memory that stores texels to be used by a texel value generating circuit, wherein said texture cache system is capable of operating in a prefetch mode such that during the rendering of a first polygon, a set of texels including at least those texels needed for completely rendering a second polygon are prefetched and stored in said texture cache memory, and wherein said set of texels are prefetched if it is determined that said set of texels can fit into one half of said texture cache memory.

105. (New) A method for processing texels, comprising:

caching a first plurality of texel values;

generating a first plurality of pixel texture values using the first plurality of cached texel values, said generating comprising reusing at least one of the first plurality of cached texel values;

defining a texture over a first triangle using the first plurality of pixel texture values;

caching a second plurality of texel values, wherein the second plurality of texel values is less in number than the first plurality of texel values; and

generating a second plurality of pixel texture values using at least one of the first plurality of cached texel values and at least one of the second plurality of cached texel values.

106. (New) The method of claim 105, further comprising defining a texture over a second triangle using the second plurality of pixel texture values.

107. (New) The method of claim 105, wherein caching the first plurality of texel values includes prefetching only the texel values necessary for defining the texture over the first triangle.

108. (New) The method of claim 105, wherein generating each of the first plurality of pixel texture values includes reading four texel values of the first plurality of cached texel values.

109. (New) A method for processing texels, comprising:

loading a cache with not more than a first plurality of texel values sufficient to define a texture of a first polygon; and

loading the cache with not more than a second plurality of texel values sufficient, when combined with the first plurality of cached texel values, to define a texture of a second polygon.

110. (New) The method of claim 109, further comprising:

generating a first plurality of pixel texture values using at least one of the first plurality of loaded texel values;

generating a second plurality of pixel texture values using at least one of the first plurality of cached texel values and at least one of the second plurality of loaded texel values;

defining the texture over the first polygon using the first plurality of pixel texture values; and

defining the texture over the second polygon using the second plurality of pixel texture values.

111. (New) A method for processing textures, comprising:

storing a plurality of texture maps in a main memory;

transferring a subset of said plurality of texture maps from the main memory to a local memory of a graphics accelerator;

accessing texels from the subset of said plurality of texture maps in the local memory; and

caching the texels in the graphics accelerator.

112. (New) The method of claim 111, wherein accessing texels includes reading page table entries, the page table entries providing physical addresses related to said plurality of texture maps.